Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A receiver for estimation and compensation of phase imbalance or gain imbalance, the receiver ~~utilizing~~ comprising:

a QPSK modulation ~~and a modulation scheme~~ circuit based on a complex scrambling code~~, the receiver comprising:~~;

a first circuit ~~that estimates~~ adapted to estimate the phase imbalance or gain imbalance of I and Q components of an incoming complex signal prior to symbol synchronization~~, using a first value related to a cross correlation of an uncompensated I component and an uncompensated Q component of an incoming I/Q modulated signal~~ the first circuit adapted to generate as outputs $I \cdot Q / I^2$ and I^2 / Q^2; and

a second circuit that receives the the uncompensated I and Q components and the outputs of the first circuit and that compensates the I and Q components of the incoming I/Q modulated signal using the outputs of the first circuit to provide compensated I and Q components for symbol synchronization.

2. (Currently Amended) The receiver according to claim 1, wherein the first circuit receives as input the I and Q components of the complex signal after demodulation~~value is a ratio between a cross correlation of said I and Q components of the incoming I/Q modulated signal and a mean value of a square of the I component, and further comprising the circuit that estimates the phase or gain imbalance using a second value that is a ratio between a cross correlation of compensated I and Q components and a square root of a product between a mean value of the square of the compensated I component and a mean value of a square of the compensated Q component, and further using a third value that is a ratio between the mean value~~

~~of the square of the compensated Q component and the mean value of the square of the compensated I component~~.

3. (Currently Amended) The receiver according to claim 1, wherein the first circuit ~~that estimates the phase imbalance or gain imbalance before synchronization~~ comprises a low pass filter for low pass filtering the signals.

4. (Canceled)

5. (Previously Presented) The receiver according to claim 1, wherein the receiver comprises a WCDMA (UMTS) receiver and wherein a feed-forward scheme or a feed-back scheme is established in the receiver.

6-20. (Canceled)

21. (New) The receiver of claim 1, wherein the first circuit comprises a multiplier that generates the a cross-correlation of the uncompensated I component and uncompensated Q components, (b) second and third multipliers that output a square of the uncompensated I and Q components, respectively, and (c) first and second dividers, the first divider outputting a ratio of the output of the first and second multipliers, and the second divider outputting a ratio of the second and third multipliers.

22. (New) A receiver for estimation and compensation of phase imbalance or gain imbalance, the receiver comprising:

a QPSK modulation circuit based on a complex scrambling code;

a first circuit adapted to estimate the phase imbalance or gain imbalance of I and Q components of an incoming complex signal prior to symbol synchronization, and first circuit adapted to generate as an output a ratio of the product of compensated I and Q components and the square of the compensated I component; and

a second circuit that receives as inputs the uncompensated I and Q components and the output of the first circuit and outputs the compensated I and Q components.

23. (New) The receiver of claim 22, wherein the first circuit receives as input the I and Q components of the complex signal after demodulation and compensation by the second circuit.

24. (New) The receiver according to claim 22, wherein the first circuit comprises a low pass filter for low pass filtering of the product of the compensated I and Q components and low pass filtering of the square of the compensated I component.

25. (New) The receiver of claim 22, comprising a synchronizer having inputs coupled to the outputs of the second circuit, the synchronizer comprising a UMTS synchronizer.

26. (New) The receiver of claim 22, wherein the first circuit comprises a first multiplier receiving the compensated I and Q signals and generating a cross correlation thereof, and a second multiplier that generates the square of the compensated I component, a divider that divides the cross-correlation of the first multiplier by the square of the compensated I component, the output of the divider integrated at an integration circuit that outputs an integration signal to the second circuit.

27. (New) A receiver for estimation and compensation of phase imbalance or gain imbalance, the receiver comprising:

a QPSK modulation circuit based on a complex scrambling code;

a first circuit adapted to estimate the phase imbalance or gain imbalance of I and Q components of an incoming complex signal prior to symbol synchronization, the first circuit adapted to generate as an output an integral of a difference between a square of a compensated I component and a square of a compensated Q component; and

a second circuit that receives the output of the first circuit and the uncompensated I and Q components and that compensate the I and Q components of the incoming signal to produce the compensated I and Q components for symbol synchronization.

28. (New) The receiver of claim 27, wherein the first circuit receives as input the I and Q components of the complex signal after demodulation and compensation.

29. (New) The receiver of claim 27, wherein the first circuit comprises a low pass filter for low pass filtering of the square of the compensated I component and the square of the compensated Q component prior to taking the difference between the square of the compensated I component and the square of the compensated Q component.

30. (New) The receiver of claim 27, comprising a WCDMA (UMTS) receiver and wherein a feed-forward scheme or a feed-back scheme is established in the receiver.

31. (New) The receiver of claim 27, further comprising a UMTS synchronizer receiving as inputs the outputs of the second circuit.

32. (New) The receiver of claim 27, wherein the first circuit comprises a first multiplier receiving the compensated Q component and generating as a product the square thereof, a second multiplier receiving the compensated I component and generating as a product the square thereof, and a subtractor circuit subtracting the product of the first multiplier from the product of the second multiplier and further comprising an integration circuit that takes the integral of the output of the subtraction circuit and outputs an integration signal to the second circuit.